ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 4, April 2015

Design of Reversible Logic ALU using Reversible logic gates with Low Delay Profile

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Abstract: Digital system implemented by using conventional gates like AND and OR gates dissipates a major amount of energy in the form of bits which gets erased during logical operations. This problem of energy loss can be solve by using reversible logic circuits in place of conventional circuits. Reversibility has become the most promising technology in digital circuits designing. In today's world ALU is one of the very important part of any system having many applications in computers, cell phones, calculators etc. In this paper the design of 1-bit reversible ALU using reversible logic gates is proposed. The proposed ALU is analyzed on FPGA SPARTAN6 device. The proposed design is compared in terms of propagation delay, quantum cost and garbage outputs. In this paper the 4-bit reversible ALU is also design on proposed 1- bit reversible ALU architecture**.**

I. INTRODUCTION

In the past decennary, great success have been made in the growth of computing machines. However, because of the exponential growth of transistor density and in particular because of the vastly increasing power dissipation, researchers expect that the conventional technologies like CMOS will reach their confines in the near future.To further fulfill the needs for more computational power, alternatives are required. In the current years, reversible logic has come out as a promising technology having its use in quantum computing, nanotechnology, low power CMOS and optical computing.The main idea of desining reversible logic are to lower the quantum cost and garbage outputs.Power dissipation is one of the most important problem in conventional technology. In 1961 landauer projected a computing device in order to bear the degrees of liberty will act as a heat sink for the energy required for calculation, resulting in computing errors.. According to Landauer's principle, the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k represents the Boltzmann's constant and value of k is 1.38x10 -23 J/K, T is the absolute temperature in Kelvin[1]. The primal combinational logic circuits dissipate heat energy for each bit of information that is lost during the operation. This is so because according to second law of thermodynamics, once the bit containing information get lost then it cannot be recovered by any approach or techniques.

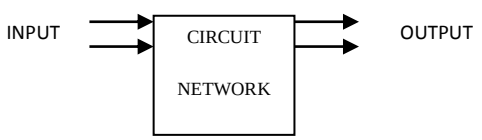
C. H. Bennett proved that the dissipated power is straightly related to the number of bits which were lost during process., and also that the computers can be reversible logically, reduced complexity and at convenient speed generate précised calculations and to avoid kTln2 joules of energy dissipation in a circuit it should be made from reversible circuits. For this the circuit must be logically reversible. A new approach of design comes in the field of digital circuits designing for limiting the power dissipation. The device designed according to this new approach is known as a *Reversible Logic Device.*

A gate designed using reversible logic is called Reversible Logic Gate. Inputs are determined by the programmers for execution in an instruction set architecture. Based on these input arithmetic logic unit should be able to generate variety of logic outputs. Hence in this type of environment reversible logic circuits must have both fixed select input lines that receive opcode signals determined by programmer and output lines where the logical output result is produce.

II. ARITHMETIC AND LOGICAL UNIT

An Arithmetic and Logic Unit (ALU) is a digital multifunctional circuit that performs Arithmetic (Sub,Add, . . .) and Logical (AND, XOR, NOR) operations on two operands A and B. In today's world ALU is very important part of any circuit or system and it have many applications in computers ,cell phones, calculators and many more. The design of low delay, low power and high speed microprocessor must consume less power. The ALU circuit must be created using reversible logic gates so that power dissipation occurs because of information loss can be ignored.

II. REVERSIBLE LOGIC GATES



DOI 10.17148/IJARCCE.2015.4477

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
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Design Verification is an important step in digital circuit design and often proves to the bottleneck in the IC development. Out of the different Design Verification areas, Functional Verification takes most of the time and effort. Equivalence Checking ensures that the design will perform required operations within the given constraints. Equivalence checking is a hard problem since the output must be as expected for all possible input vectors, which might be exponential to the number of inputs. There are two main classes of Equivalence Checking :-One is equivalence checking done on simulation based and second is the Equivalence checking done on formal based.. Simulation-based Equivalence Checking, is a straight-forward checking but presents many challenges. It needs creation of test benches for various input states. Also, a There are three basic 2x2 reversible logic gates. The Controlled-Not gate [4] – commonly called the Feynman gate - is designed to produce the following output states: P = X and Q = X xor Y. Since fanout is expressively forbidden in reversible logic, since a fanout has one input and two outputs, the Feynman gate can be used to duplicate a signal when Y is equal to 0. Quantum cost of Fynman gate is 1..

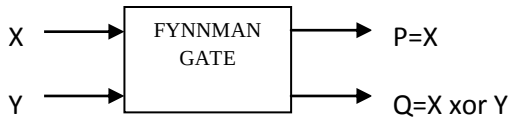

Figure 2.1: Block Diagram of Feynman Gate

In the reversible logic, a XOR gate can be represented as shown in Fig. 2.2, where A, B and P, Q are the input and output vectors respectively. Here the mapping between theinputs and outputs can be represented as P = A and Q = A $\otimes$ B .The reconstruction of input vectors from the output vectors can be seen in table 2.1. In the table 2.1 each output vector corresponds to a unique input vector.

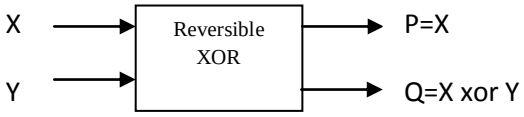

Figure. 2.2. Reversible XOR gate

Table 2.1. Truth table of reversible XOR gate

A	B	P = A	Q =A $\otimes$ B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

R is a 3*3 reversible gate whose block diagram is shown in fig.2.3. Having inputs (X,Y,Z) and outputs P=X xor Y; Q= X and R=Z' xor XY. . Quantum cost of R gate is 4.

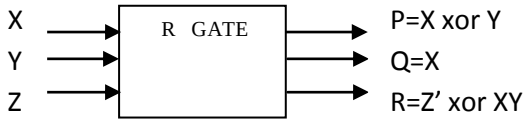

Figure.2.3. Block Diagram of R Gate

BME is a 4*4 reversible gate whose block diagram is shown in fig.2.4. Having inputs (X,Y,Z,T) and outputs P=X ', Q=XY xor Z , R=XT xor Z and S=X' Y xor Z xor T . Quantum cost of BME gate is 6.

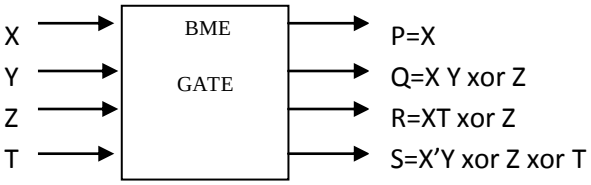

Figure. 2.4. Block Diagram of BME Gate

The DKG gate is a 4*4 reversible gate whose block diagram is shown in fig.2.5. Having inputs (X,Y,Z,T) and outputs are P=Y, Q= X'Z+XT , R= X xor Y) (Z xor T)Zxor ZT and S=Y xor Z xor T. Quantum cost of DKG gate is 6. This gate can be used as a half adder as well as a full adder. This gate is designed from Peres gate..

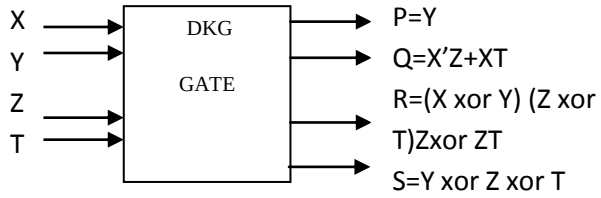

Figure. 2.5. Block Diagram of DKG Gate

Quantum technology is essentially reversible and is one of the important promising technologies for future computing systems. In addition to reversibility, it has unique features such as quantum superposition, quantum parallelism and quantum entanglement that allows for solving problems much more powerfully than in classical computing. (Observe that the quantum circuit is reversible when it calculates in Hilbert Space before the measurement. It is no longer reversible after measurement, since the probabilistic measurement cannot be reversed). Although only a few quantum algorithms are known in 2010, many problems can be reduced to some of these algorithms, for instance to the Quantum Fast Fourier Transform or to Grover's algorithm. Thus, any NP-hard problem can be reduced to Grover's algorithm to give a practically useful and substantial

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 4, April 2015

reduction in complexity for large values of N. This reduction is, however, not as high as in the case of the exponential speedup obtained by the famous Shor's quantum algorithm for integer factorization.

To design an efficient reversible circuit, analysis of the programmability of the logic device the number of logical calculations produced on the fixed outputs should be considered in addition to the quantum cost and delay. The BME, R, FEYNMAN, DKG, MRG and the HNG are very efficient gates, because they produce the greatest number of logical calculations at the lowest cost.

Table 2.2. Cost and Logical outputs of Reversible logic gates

GATES	COST	LOGICAL OUTPUTS
FYNMAN	1	X xor Y
R	4	XxorY, XY
DKG	6	XxorY, X+Y, (X+Y)',
BME	6	XxorY, (XY)', XY, X'

III. PROPOSED METHODOLOGY

The basic part of the arithmetic segment of the ALU is a parallel adder. A parallel adder is builded with a number of full adders and the proposed 1-bit and 4-bit reversible ALU utilizes DKFG gate as full adder By scheming the data inputs to the parallel adder, it is likely to get different type of operations. Input carry CIN enters to the full adder gate in the least important bit position and exists out as COUT from the adder. Sums are gets from the outputs of the full adder. The arithmetic addition is realized when one set of input enters through the A inputs and the other set enters through the B inputs and the input carry is keep as 0. When CIN =1 it is possible to add 1 to the sum in Functions, if we complement all the bits of B then we will get F= (A+B) . And when CIN= ! we will get F= (A-B). Similarly if all inputs of B is 0, we get the transfer A function. The proposed 1 and 4-bit ALUs is shown in figure 2.6. and logical outputs based on inputs opcodes are shown in Table 2.3.(a) and (b).

Table 2.3 (a).Proposed 1-Bit ALU Opcodes

S0	S1	S2	S3	S4	CIN	OPERATIONS	FUNCTIONS
0	0	0	0	0	0	F=X	Transfer X
0	0	0	0	0	1	F= X+Y	Addition
0	0	1	0	1	0	F= X+Y'+1	Subtract
0	0	0	0	1	1	F= X $\otimes$ Y	XOR
1	0	0	1	0	0	F= X ^ Y	OR
0	0	0	1	0	1	F= X & Y	AND
0	0	0	1	1	0	F= X'	NOT
0	1	0	1	1	1	F= (X &Y)'	NAND

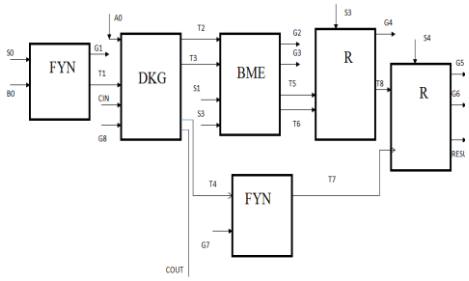

Fig. 2.6 (a). Reversible 1-bit ALU

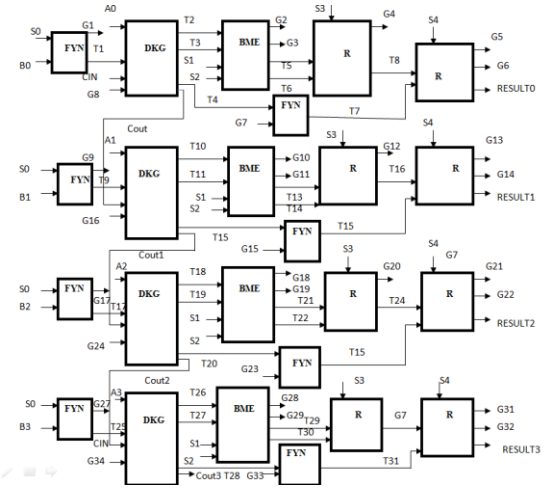

Fig. 2.6 (b). Reversible 4-bit ALU

Table 2.3(b). Proposed 4-Bit ALU Opcodes

S0	S1	S2	S3	S4	CIN	OPRATIONS	FUNCTIONS
0	0	0	0	0	0	F = X	Transfer X
0	1	0	0	0	0	F = X+1	Increment X
0	0	0	0	0	1	F = X+Y	Addition
0	0	1	0	1	0	F = X+Y'+1	Subtract
1	0	0	1	0	0	F = X-1	Decrement X
0	0	0	0	1	1	F = X $\otimes$ Y	XOR
1	0	0	1	0	0	F = X^ Y	OR
0	0	0	1	0	1	F = X& Y	AND
0	0	1	0	0	0	F = X'	NOT
0	0	0	1	1	0	F =(X $\otimes$ Y)'	XNOR
0	0	0	1	1	0	F= (X& Y)'	NAND
0	1	0	0	1	0	F =(X ^ Y)'	NOR

The proposed 4-Bit ALU is higher in terms of delay, quantum cost than the proposed 1-Bit ALU. The presented ALUs has two most important advantages. First, it produces less delay than the existing 1-Bit logic architecture. As a result, the proposed ALU has a better

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 4, April 2015

quantum delay for n-bit ALUs. Second, proposed ALU produces more arithmetic and logical operations. The proposed ALU is designed to be flexible so that any alterations required for implementation in an instruction set architecture will be easy.

IV. SIMULATION RESULTS

The proposed 1-bit and 4-bit ALU architecture presented and explained in the previous section is synthesized and simulated on XILINX ISE. The simulation waveforms of both 1 and 4-bit ALUs are shown in figure.2.7(a) and (b.)

Fig. 2.7 (a). Simulation waveform of Reversible 1-bit ALU

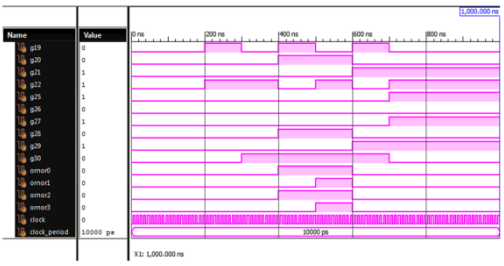

Fig. 2.7 (b). Simulation waveform of Reversible 4-bit ALU

Table 2.4 show the performance comparison of the existing ALU design with the proposed reversible ALU designs. For comparison, propagation delay, ,quantum cost and garbage output are considered as the performance matrices.

Parameter which has to be compared	Proposed 4-bit reversible ALU	Proposed 1-bit reversible ALU	Eixting 1-bit reversible ALU
Delay	7.885ns	6.334ns	16ns
Quantum Cost	88	22	24

Table 2.4. Comparison between the proposed reversible 1 and 4-bit ALU Designs with the existing 1- bit ALU design

V. CONCLUSION

The programmable reversible gates have been studied in reversible arithmetic logic units. These new ALU designs are advantageous to previously published work in implementations that favor low delay and high logical calculation output, which is desirable for realization of a reversible central processing unit. The proposed designs can be integrated in the design of a n-bit reversible arithmetic logic unit. In this paper investigation and analysis done on gates on FPGA SPARTAN6 device. With the above analysis it can also be derived that proposed 1-Bit ALU has Less delay than the existing 1-Bit ALU. The quantum cost and garbage is also small to design a 32-Bit ALU. For conventional logic circuits there exist much research, even whole books, dedicated to the design and simulation of computer arithmetic. This is definitely not the case for reversible logic. The constraint that the circuits must be garbage-free is what makes it an interesting research problem, but most proposed designs still implement the conventional algorithms with garbage. They use the reversible gates, but as their sole goal is to reduce logic size or number of garbage bits for a specific fixed-size circuit, very little knowledge is actually gained from this approach.

REFERENCES

[1] Morrison, M.; Ranganathan, N., "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," VLSI (ISVLSI), 2011 IEEE Computer Society Annual Symposium on , vol., no., pp.126,131, 4-6 July 2013

[2] Sharma, S.; Singh, S.B.; Akashe, S., "Optimized power performance and simulation of reversible logic multiplexer," Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), 2013 Annual International Conference on , vol., no., pp.1,6, 4-6 June 2013.

[3] Roohi, A.; Khademolhosseini, H.; Sayedsalehi, S.; Navi, K., "Implementation of reversible logic design in nanoelectronics on basis of majority gates," Computer Architecture and Digital Systems (CADS), 2012 16th CSI International Symposium on , vol., no., pp.1,6, 2-3 May 2012.

[4] Sayem, A.S.M.; Mitra, S.K., "Efficient approach to design low power reversible logic blocks for Field Programmable Gate Arrays," Computer Science and Automation Engineering (CSAE), 2011 IEEE International Conference on , vol.4, no., pp.251,255, 10-12 June 2011.

[5] Banerjee, A.; Das, D.K., "Squaring in reversible logic using iterative structure," Design & Test Symposium (EWDTS), 2014 East-West , vol., no., pp.1,4, 26-29 Sept. 2014.

[6] Jagannatha, K.B.; Divya, D.; Reddy, K.S.; Desai, P.K.; Sevanthi, S., "ASIC design of reversible full adder circuits," Computing, Electronics and Electrical Technologies (ICCEET), 2012 International Conference on , vol., no., pp.734,737, 21-22 March 2012.

[7] Nagamani, A.N.; Ashwin, S.; Agrawal, V.K., "Design of optimized reversible binary adder/subtractor and BCD adder," Contemporary Computing and Informatics (IC3I), 2014 International Conference on , vol., no., pp.774,779, 27-29 Nov. 2014.

[8] Kaur, P.; Dhaliwal, B.S., "Design of fault tolearnt full Adder/Subtarctor using reversible gates," Computer Communication and Informatics (ICCCI), 2012 International Conference on , vol., no., pp.1,5, 10-12 Jan. 2012.

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 4, April 2015

[9] Banerjee, A., "Reversible cryptographic hardware with optimized quantum cost and delay," India Conference (INDICON), 2010 Annual IEEE , vol., no., pp.1,4, 17-19 Dec. 2010.
[10] Md Hasan Babu, H.; Saleheen, N.; Jamal, L.; Sarwar, S.M.; Sasao, T., "Approach to design a compact reversible low power binary comparator," Computers & Digital Techniques, IET , vol.8, no.3, pp.129,139, May 2014.
[11] Nagamani, A.N.; Ashwin, S.; Agrawal, V.K., "Design of optimized reversible Binary and BCD adders," VLSI Systems, Architecture, Technology and Applications (VLSI-SATA), 2015 International Conference on , vol., no., pp.1,5, 8-10 Jan. 2015.
[12] Khurana, S.; Grover, A.; Grover, N., "Comparative Analysis: Power Reversible Comparator Circuits 90 Nm Technology," Modelling Symposium (AMS), 2013 7th Asia , vol., no., pp.103,107, 23-25 July 2013.
[13] Grover, A., "Design of Power Reversible Comparators with Different Technologies," Computational Intelligence, Modelling and Simulation (CIMSim), 2013 Fifth International Conference on , vol., no., pp.193,196, 24-25 Sept. 2013.
[14] Yeh, P.-Y.; Ye, B.-Y.; Kuo, S.-Y.; Chen, I.-Y., "Effective design-for-testability techniques for H.264 all-binary integer motion estimation," Circuits, Devices & Systems, IET , vol.4, no.5, pp.403,413, September 2010.
[15] Lisa, N.J.; Babu, H.M.H., "A compact realization of a reversible quantum n-to-2^n decoder," Electronics Information and Emergency Communication (ICEIEC), 2013 IEEE 4th International Conference on , vol., no., pp.90,93, 15-17 Nov. 2013.